Flight Computer Infrastructure Capabilities for Deep-Space Landed Missions

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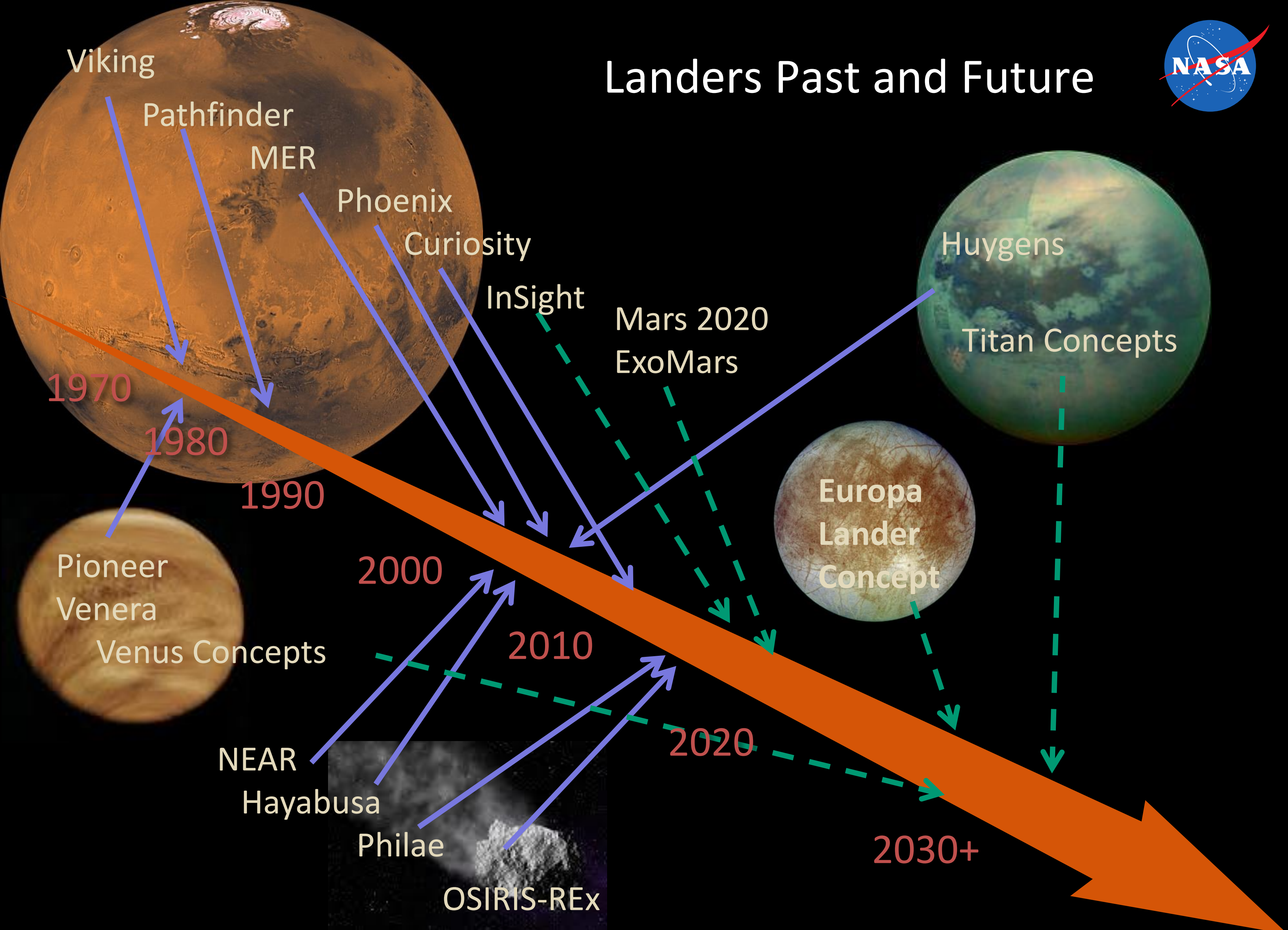
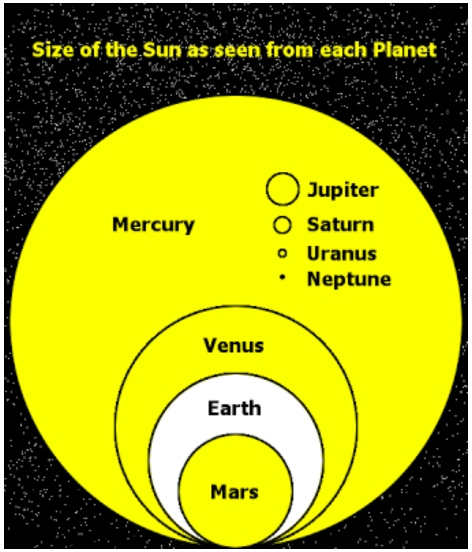
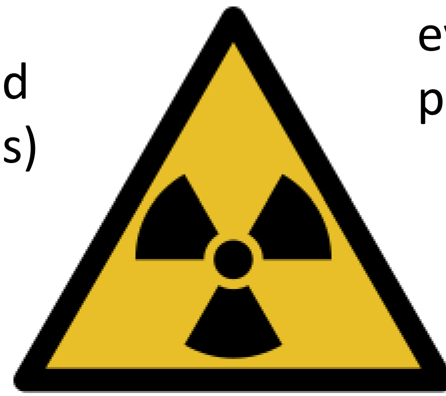


Predecisional information for planning and discussion only

Constraints: Extreme Environments

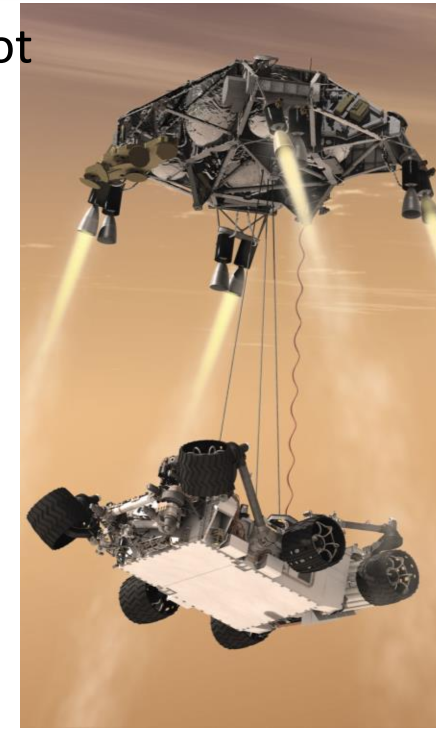


Diminishing solar energy available (and diurnal cycles)

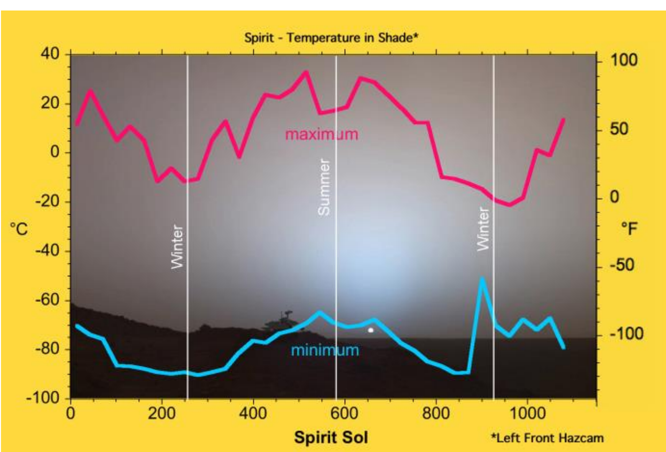


Severe transient and total dose radiation effects

One-shot critical events/ phases

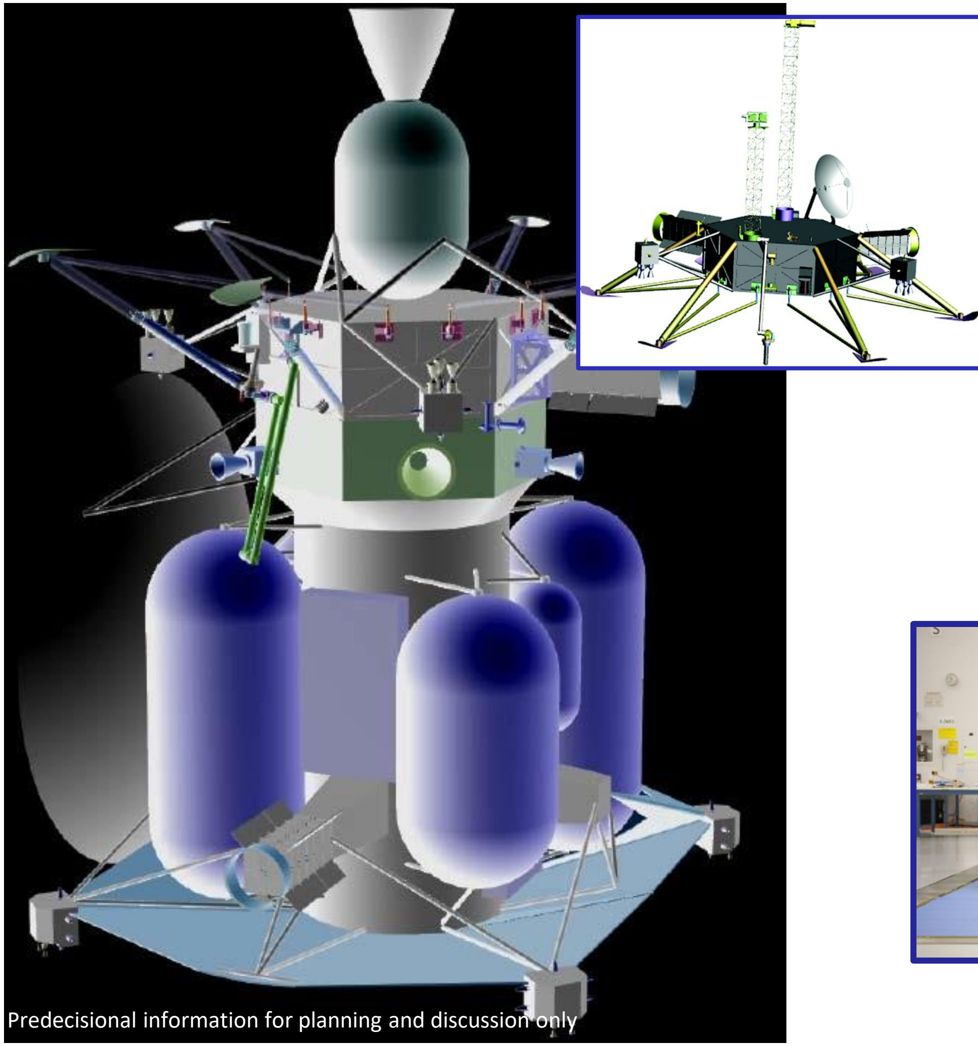


Deep diurnal temperature variance

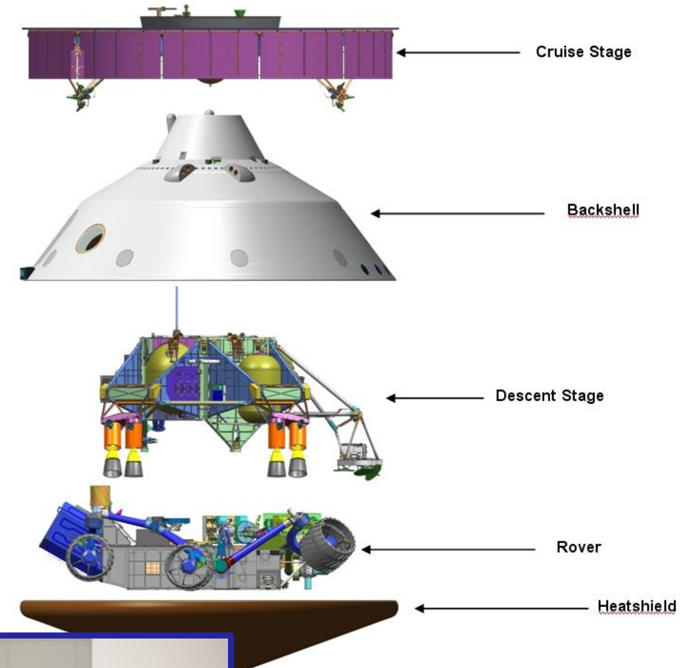


Limited and high-latency communications

Constraints: Mass and Volume

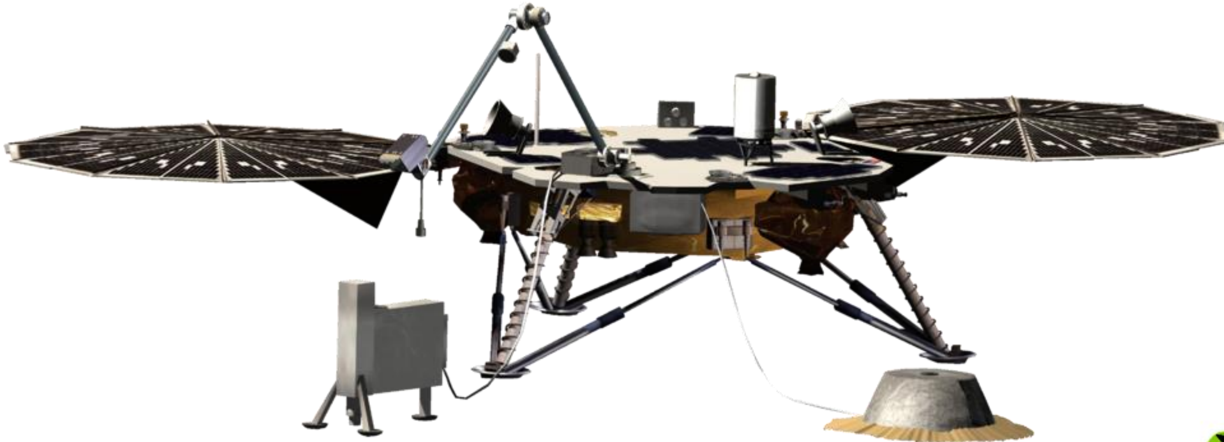


Europa concept mass: Est 10% of launch weight
Launch vehicle: SLS

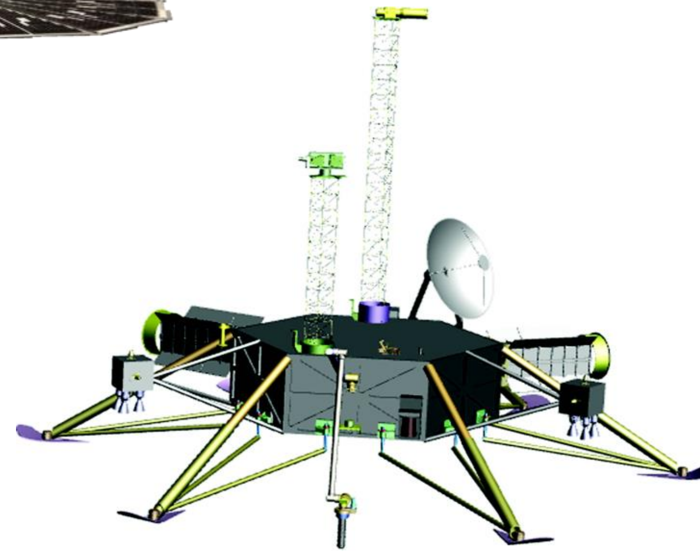


Mars 2020 rover mass: 25% of launch weight
Launch Vehicle: ATLAS 5

Constraints: Long Project Lifecycles



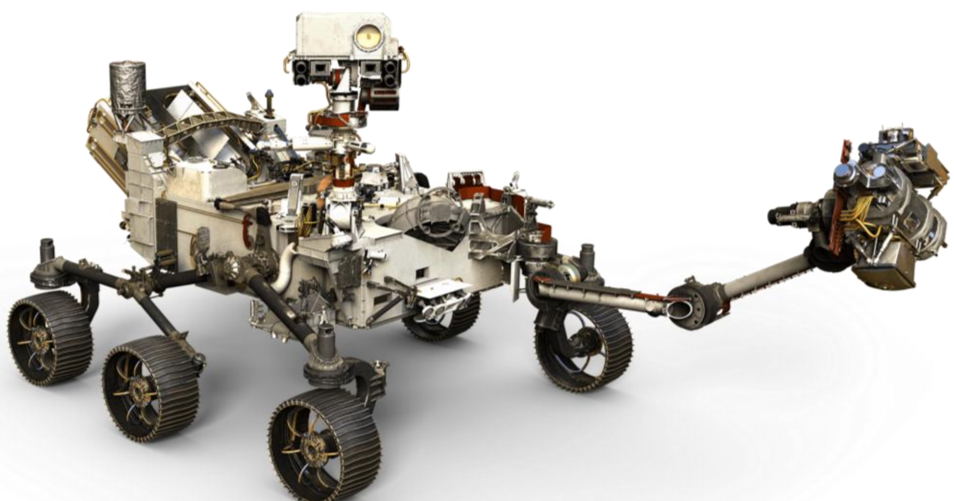
Insight (2018) - 2003 start (Phoenix)



Europa Concept (Est 2024)

- 2014 study start
- Proposed 8 year Cruise

Predecisional information for planning and discussion only

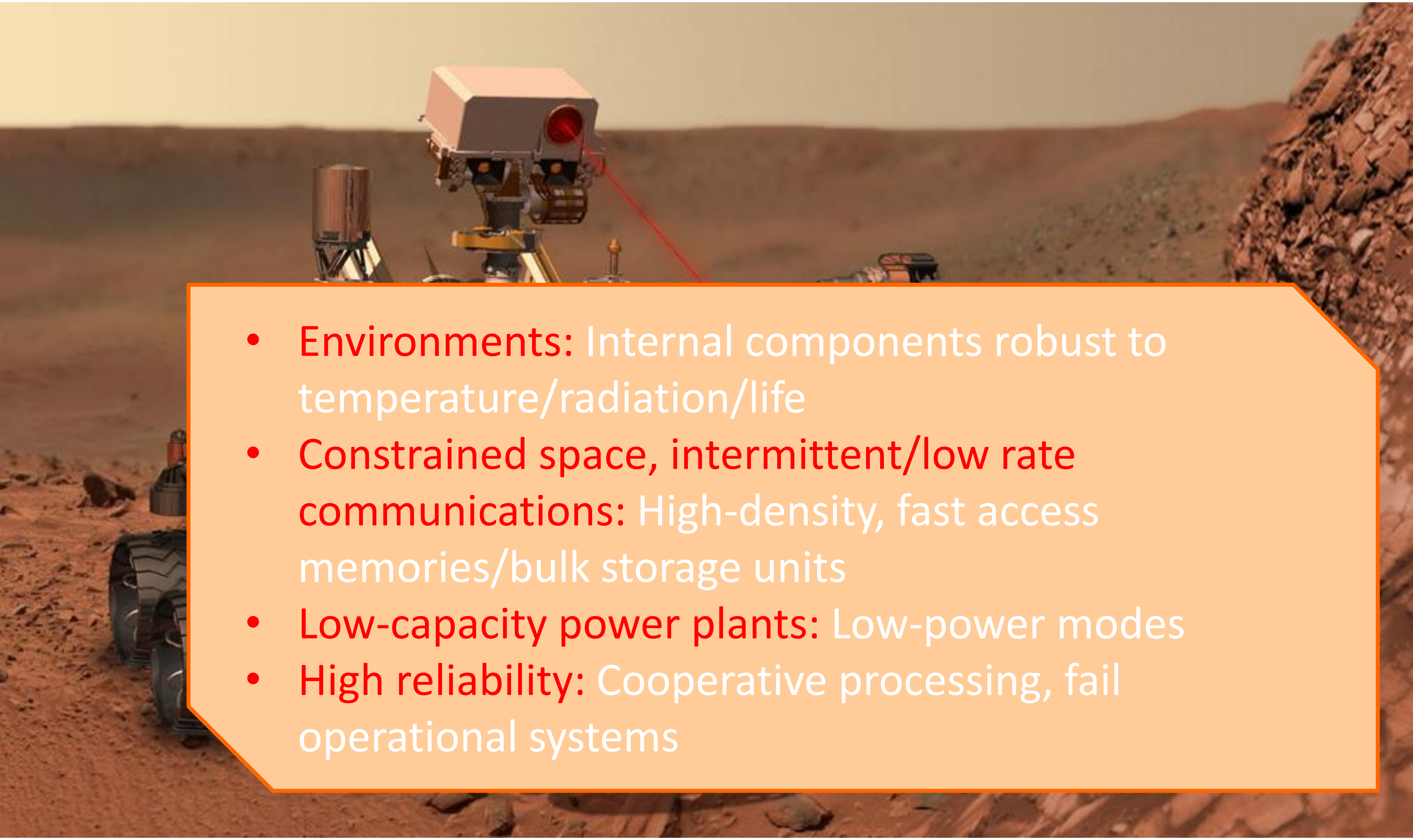


Mars 2020 (2020) - 2004 start (Curiosity)

Unique Lander Missions = Custom Payloads

Cameras (Mars 2020 has 23!) -- context, composition
Spectrometer/Chromatograph -- composition
Radar/LIDAR -- topology, including subsurface
Laser/X-ray -- elemental/molecular composition
Magnetometers/Particle Detectors -- fields, flux
Seismometers -- seismic motion
Mechatronics -- deployments/surface sampling

Computing Priorities for Landers



- **Environments:** Internal components robust to temperature/radiation/life
- **Constrained space, intermittent/low rate communications:** High-density, fast access memories/bulk storage units
- **Low-capacity power plants:** Low-power modes
- **High reliability:** Cooperative processing, fail operational systems

JPL Processor Architectures

"Flagship" Missions

- Backplane-based space-qualified computer
  - E.g. GVSC-1750, RAD 6000, RAD 750
  - Often developed with government support
  - Substantial need for custom interface cards
- Bulk Storage Memory
  - Low availability of space flash/sdram
  - Low access speeds

Smaller Missions

- Custom compute board built around space-qualified processor
  - E.g. SPARC, Leon, FPGA/embedded cores
  - May be used in highly constrained/customized applications
- Memory
  - Reprogrammability helps mitigate long lifecycles
  - New robust technologies (CRAM/MRAM) still low density

JPL Interface Topologies

- 1553 still widely used
  - Robust and proven
  - Slow and inflexible
- Payload interfaces generally point-to-point
  - Resource-intensive
  - Lack of available standardized bus interface parts/drivers
- Cabling mass/volume significant contributions
- Deployments and cruise-to-landed configuration changes require safely cutting interfaces

JPL Current Research Efforts

- Software architectures for multicore and fail-operational computing
- Advanced commercial parts screening and packaging techniques
- Robust multipoint bus architectures
- Adaptive data compression and management strategies

Curiosity flight computers